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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/872,091	06/01/2001	Yasuteru Araya	14669	2464

23389 7590 01/18/2006

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EXAMINER

THANGAVELU, KANDASAMY

ART UNIT PAPER NUMBER

2123

DATE MAILED: 01/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/872,091

Applicant(s)

ARAYA ET AL.

Examiner

Kandasamy Thangavelu

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 December 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 11-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 11-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 December 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 12 October 2005.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to the Applicants' Amendment dated December 9, 2005. Claims 11-13 and 16 were amended. Claims 11-19 of the application are pending. This office action is made final.

Information Disclosure Statement

2. Acknowledgment is made of the information disclosure statement filed on October 12, 2005. The paper provided with the information disclosure statement has been considered in reviewing the claims.

Drawings

3. The drawing for Figure 1 submitted on December 9, 2005 is accepted.

Specification

4. The disclosure is objected to because of the following informalities:

In specification Page 2, Line 2, "simulation platform" should be "simulation program".

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In specification Page 9, Line 21, " so that the simulation platform is to be structured again " appears to be incorrect and it appears that it should be "so that the simulation program is structured again".

Specification Page 9, Line 22, "Fig. 3 shows an example of the 'restructured' simulation platform" appears to be incorrect and it appears that it should be "Fig. 3 shows an example of the 'restructured' simulation program".

Appropriate corrections are required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. §112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 11-19 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In the paragraphs below, ***new material*** refers to the material added in the amendment of November 26, 2004.

6.1 Claim 11, Lines 4-6 state, “structuring source code describing the algorithm design in a general purpose high-level programming language by isolating elements of said source code representing hardware units and software units” and Lines 12-13 state, “performing said performance evaluation by simulating said modified source code elements and counting said data traffic on the bus”.

Specification Page 2, Lines 1-7 state, “Prior to actual manufacturing, simulation programs (or algorithms) are normally structured without consideration of distinctions between hardware and software... Next, isolation of hardware and software is performed on the structured simulation programs, which are divided into hardware elements and software elements of the simulation program respectively. The isolation of hardware and software is made by experimentation”. The specification does not describe how the simulation programs are structured and how this structuring affects isolation of the hardware and software.

Specification Page 6, Lines 22-25 state, “a simulation program is structured to perform architecture design by using sources ...in simulation program structuring process, the flow proceeds to step A3 to effect isolation of hardware and software”. Therefore it is understood that structuring the simulation program involves isolation of the hardware and software.

The simulation program is a software tool and it is not hardware. Therefore the structuring of simulation platform involving *isolation of hardware and software* mentioned in Specification, Page 6, Lines 22-25 is not understood.

One of ordinary skill in the art will understand that bus operations involve both bus hardware and bus operational software. There is much interaction between hardware and software. Any simulation model of the bus operation will involve both the hardware models and

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the software models. Therefore it is not understood as to why one will isolate hardware and software in any simulation model of bus operations and how it will affect the simulated bus performance.

It is also not understood as to how “The isolation of hardware and software is made by experimentation”. The specification does not state as to what criteria and process are used to isolate the hardware and software during structuring the simulation program. Therefore the process of structuring the simulation program is not properly described in the specification.

In view of the lack of proper description of the structuring process in the specification, “structuring source code describing the algorithm design in a general purpose high-level programming language by isolating elements of said source code representing hardware units and software units” is not understood.

In addition, the statement, “isolating elements of said source code representing hardware units and software units” is *new material* not found in the original specification and therefore this amendment to the claim is not allowed.

6.2 Claim 14 refers to, “feeding back a result of the performance evaluation of the bus to the step of structuring the source code to improve the architecture design at a high-level design stage by isolating in said source code new elements representing hardware units and new elements representing software units”. The process of structuring the source code is not properly described in the specification, as explained in Paragraph 6.1 above.

In addition, the statement, “isolating in said source code new elements representing hardware units and new elements representing software units” is *new material* not found in the original specification and therefore this amendment to the claim is not allowed.

6.3 Claim 15 refers to “isolation of the source code into elements representing hardware units and elements representing software units”. This is *new material* not found in the original specification and therefore this amendment to the claim is not allowed.

6.4 Claim 16, Lines 12-14 refer to, “structuring the source code into elements representing at least one of the hardware units and the software units for use in the architecture design by compiling said source code”. The process of structuring the source code is not properly described in the specification, as explained in Paragraph 6.1 above.

In addition, the statement, “into elements representing at least one of the hardware units and the software units” is *new material* not found in the original specification and therefore this amendment to the claim is not allowed.

6.5 Claims rejected but not specifically addressed are rejected based on their dependency on rejected claims.

7. Claim 15 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

7.1 Claim 15 states, “in response to the bus traffic, isolation of the source code into elements representing hardware units and elements representing software units is optimized”. The specification does not describe anywhere how this isolation of the source code in elements representing hardware units and elements representing software units is optimized. It does not describe the objective function and the process used for optimization of isolation of the source code into elements representing hardware units and elements representing software.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 11-15 and 17-19 are rejected under 35 U.S.C. 102(a) and 102(b) as being anticipated by **Tammemaie et al.** (“AKKA: A tool for cosynthesis and prototyping”, The Institution of Electrical Engineers, UK, 1996).

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9.1 **Tammemae et al.** teaches AKKA: A tool for cosynthesis and prototyping. Specifically, as per claim 11, **Tammemae et al.** teaches a method in a LSI design and development process (Page 1, Para 1, L1-2; Page 1, Para 2, L2-5), for evaluating an architecture design for an algorithm design by performing a performance evaluation of at least one bus at a high-level stage of the design and development process (Page 1, Para 2, L2-4; Page 1, Para 4, L2; Page 2, Para 4, L3); the method comprising:

structuring source code describing the algorithm design in a general purpose high-level programming language (Page 1, Para 2, L2-3; Page 1, Para 3, L1-3), by isolating elements of the source code representing hardware units and software units (Page 1, Para 2, L3; Page 1, Para 3, L7-8; Page 3, Fig. 1);

creating an evaluation function for counting data traffic that occurs on the at least one bus (Page 1, Para 4, L2; Page 1, Para 2, L3-4; Page 2, Para 4, L3; Page 3, Fig. 1; Page 2, Para 2, L4), the bus being a part of the source code realizing the data traffic between the elements representing hardware units and software units (Page 1, Para 4, L2; Page 1, Para 2, L3-4; Page 1, Para 5, L5-6; Page 2, Para 2, L4);

modifying at least one element of the source code elements based on a result of an implementation of the evaluation function (Page 2, Para 5, L1-3; Page 2, Para 4, L3; Page 2, Para 2, L4); and

performing the performance evaluation by simulating the modified source code elements and counting the data traffic on the bus (Page 2, Para 5, L1-3; Page 3, Fig. 1; Page 4, Para 1, L2-3).

Per claim 12: **Tammemae et al.** teaches restructuring the source code based on the evaluated data traffic (Page 1, Para 2, L3-4; Page 1, Para 4, L1-2); and

performing the performance evaluation again by simulating the restructured source code again (Page 2, Para 5, L1-3; Page 3, Fig. 1; Page 4, Para 1).

Per claim 13: **Tammemae et al.** teaches that a bus traffic is calculated from the evaluated data traffic with respect to the processing rate of the bus (Page 2, Para 5, L1-3).

Per claim 14: **Tammemae et al.** teaches feeding back a result of the performance evaluation of the bus to the step of structuring the source code to improve the architecture design at a high-level design stage by isolating in the source code new elements representing hardware units and new elements representing software units (Page 1, Para 2, L3-4; Page 1, Para 4, L1-2; Page 2, Para 5, L1-3).

Per claim 15: **Tammemae et al.** teaches that in response to the bus traffic, isolation of the source code into elements representing hardware units and elements representing software units is optimized (Page 1, Para 2, L3-4; Page 1, Para 4, L1-2; Page 2, Para 5, L1-3).

Per claim 17: **Tammemae et al.** teaches that the variables loaded onto the bus consist of n bits while the bus consists of m bit lines, where n and m are both integers, and n is a multiple of m , and the bus traffic for the processing rate is produced such that the number of times in effecting data transfer on the bus is multiplied by n/m and is then divided by the processing rate

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(Page 2, Para 5, L1-3). **Tammemae et al.** teaches that each variable access is counted using a counter and a log of the access of the variables is made. It is inherent that from the counting of the variable access to a bus, and the log of the variable accesses, it is possible to calculate the number of times the bus was used if the bus width was smaller than the variable length requiring multiple accesses to the bus for each variable loaded onto the bus.

Per claim 18: **Tammemae et al.** teaches that the general purpose high-level language is one of C language and C++ language (Page 1, Para 2, L2-3; Page 1, Para 3, L1-3).

Per claim 19: **Tammemae et al.** teaches that the evaluation function increments a counting value if a pre-defined variable is loaded onto the bus (Page 2, Para 5, L1).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

11. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

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1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Tammemae et al.** ("AKKA: A tool for cosynthesis and prototyping", The Institution of Electrical Engineers, UK, 1996) in view of **Raimi et al.** (U.S. Patent 5,604,895) and **Adams et al.** ("Execution time profiling for multiple process behavioral synthesis", IEEE, 1995).

12.1 As per claim 16, **Tammemae et al.** teach the method of claim 11. **Tammemae et al.** teaches creating the evaluation function (Page 1, Para 4, L2; Page 1, Para 2, L3-4; Page 2, Para 4, L3; Page 3, Fig. 1; Page 2, Para 2, L4);

profiling the source code based on whether a line of source code represents writing data to variables that are defined in advance and are loaded onto the bus to be evaluated (Page 2, Para 4, L3; Page 2, Para 2, L4);

structuring the source code into elements representing at least one of the hardware units and the software units for use in the architecture design by compiling the source code (Page 1, Para 2, L3; Page 1, Para 3, L7-8; Page 3, Fig. 1);

calculating the data transfer rate on the bus by executing the compiled source code elements in a simulation program (Page 2, Para 5, L1-3; Page 3, Fig. 1; Page 4, Para 1, L2-3);

calculating bus traffic with regard to a given processing rate of the bus (Page 2, Para 5, L1-3); and

performing evaluation of the performance of the bus in response to the bus traffic (Page 2, Para 5, L1-3; Page 3, Fig. 1; Page 4, Para 1, L2-3).

Tammemae et al. does not expressly teach after creating the evaluation function, sequentially reading in the source code line by line while effecting syntax analysis; determining whether the source code is to be modified based on whether a line of source code represents writing data to variables that are defined in advance and are loaded onto the bus to be evaluated; upon determining that the source code is to be modified, modifying the source code by embedding the evaluation function one of immediately before or immediately after the line of source code in which the variable is written; and repeating the forgoing steps until the source code is completely read in up to a last line of source code. **Raimi et al.** teaches after creating the evaluation function, sequentially reading in the source code line by line while effecting syntax analysis (Abstract, L5-6; CL2, L20-22); determining whether the source code is to be modified based on whether a line of source code represents writing data to variables that are defined in advance and are loaded onto the bus to be evaluated (CL1, L26-32; CL1, L64-66; CL2, L37-54); upon determining that the source code is to be modified, modifying the source code by embedding the evaluation function one of immediately before or immediately after the line of source code in which the variable is written (CL1, L26-32; CL1, L64-66; CL2, L23-29; CL2, L37-54); and repeating the forgoing steps until the source code is completely read in up to a last line of source code (Abstract, L5-6; CL2, L20-22). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Tammemae et al.** with the method of **Raimi et al.** that included after creating the evaluation function,

sequentially reading in the source code line by line while effecting syntax analysis; determining whether the source code was to be modified based on whether a line of source code represented writing data to variables that were defined in advance and were loaded onto the bus to be evaluated; upon determining that the source code was to be modified, modifying the source code by embedding the evaluation function one of immediately before or immediately after the line of source code in which the variable was written; and repeating the forgoing steps until the source code was completely read in up to a last line of source code because that would allow generation of additional code to check for the occurrence of bus access events (CL1, L65-66)..

In addition, **Adams et al.** teaches after creating the evaluation function, sequentially reading in the source code line by line while effecting syntax analysis; determining whether the source code is to be modified based on whether a line of source code represents writing data to variables that are defined in advance and are loaded onto the bus to be evaluated; upon determining that the source code is to be modified, modifying the source code by embedding the evaluation function one of immediately before or immediately after the line of source code in which the variable is written; and repeating the forgoing steps until the source code is completely read in up to a last line of source code (Page 144, Fig. 1; Abstract, L1-3; Page 145, CL1, Para 2), because that results in a simulation model that has the same cycle-by-cycle behavior as the RTL model but can be simulated in a fraction of the time (Abstract, L4-6); it allows performance of the system to be evaluated dynamically, by simulating the system, using a simulation model that accurately reflects the results of behavioral synthesis (Page 144, CL1, Para 3, L7-10).

Response to Arguments

13. Applicants' arguments with respect to 35 USC 112 first Paragraph, 112 second Paragraph, 35 USC 102 (a) and (b) and 35 USC 103 (a) rejections filed on December 9, 2005 have been considered. Applicants' arguments with respect to 35 USC 112 first Paragraph and 35 USC 102 (a) and (b) and 35 USC 103 (a) rejections are not persuasive.

13.1 As per the applicants' argument that "isolation of hardware and software elements is properly described in the specification at Page 2, lines 5-7; additionally, the isolation of the hardware and software elements is performed by experimentation since this is an iterative process during the architectural design of the LSI device; the optimization will vary with respect to the aims of each hardware/software architecture designer according to varied design factors (i.e. hardware expertise, software expertise, budget, speed of hardware design, etc.)", the Examiner takes the position that specification Page 2, Lines 5-7 does not describe how the simulation programs are structured and what rules and criteria are used to structure the simulation programs; it does not describe how the simulation programs are isolated into hardware and software using experimentation – what procedure or process is used to isolate the hardware and software. If the applicants claim that the "the optimization will vary with respect to the aims of each hardware/software architecture designer according to varied design factors", then this process is well known to one of ordinary skill in the art. Therefore, the applicants cannot claim such elements which are well known to one of ordinary skill in the art.

13.2 As per the applicants' argument that "Applicants respectfully traverse the new matter rejection with respect to claim 14; support for the limitation can be found, for example, in the specification Page 10, lines 11-15; Applicants respectfully submit that the optimization will vary with respect to the aims of each hardware/software architecture designer according to varied design factors (i.e. hardware expertise, software expertise, budget, speed of hardware design, etc.)", the Examiner takes the position that the new material not allowed by the Examiner refers to "isolating in said source code new elements **representing** hardware units and new elements representing software units" and "isolation of the source code into elements **representing** hardware units and elements representing software units is optimized". This source code representing hardware elements and source code representing software elements is not found in the original specification at Page 10, Lines 11-15 and Page 2, Lines 5-7.

13.3 As per the applicants' argument that "the isolation of the hardware and software elements is performed by experimentation since this is an iterative process during the architectural design of the LSI device; the optimization will vary with respect to the aims of each hardware/software architecture designer according to varied design factors (i.e. hardware expertise, software expertise, budget, speed of hardware design, etc.); it is well settled that an "inventor need not, however, explain every detail since he is speaking to those skilled in the art"; additionally, "not every last detail is to be described, else patent specifications would turn into production specifications, which they were never intended to be"", the Examiner takes the position that if the applicants claim that the "the optimization will vary with respect to the aims of each hardware/software architecture designer according to varied design factors", then this process is

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well known to one of ordinary skill in the art. Therefore, the applicants cannot claim such elements which are well known to one of ordinary skill in the art.

13.4 As per the applicants' argument that "Tammemae is directed to a toolkit for the co-synthesis and prototyping of re-configurable and dedicated hardware; Tammemae teaches including data transfer profiling, such that for each variable access by the hardware element, a call to a counter function is made, and thereby each variable access is kept track of and counted; Tammemae does not disclose or suggest a software bus between the hardware and software elements of the simulation to exchange data traffic as required by claim 11; since Tammemae does not disclose the software bus, Tammemae additionally fails to disclose counting the data traffic on the bus; the cited reference does not disclose each and every limitation recited in the amended claims", the Examiner respectfully disagrees. Tammemae teaches software modeling of the hardware and software elements of design for hardware/software co-simulation. The data transfer between the hardware elements and the software elements is modeled as part of the interface between the two. The bus in the software model is a software bus.

Tammemae teaches creating an evaluation function for counting data traffic that occurs on the at least one bus (Page 1, Para 4, L2; Page 1, Para 2, L3-4; Page 2, Para 4, L3; Page 3, Fig. 1; Page 2, Para 2, L4), the bus being a part of the source code realizing the data traffic between the elements representing hardware units and software units (Page 1, Para 4, L2; Page 1, Para 2, L3-4; Page 1, Para 5, L5-6; Page 2, Para 2, L4);

modifying at least one element of the source code elements based on a result of an implementation of the evaluation function (Page 2, Para 5, L1-3; Page 2, Para 4, L3; Page 2, Para 2, L4); and

performing the performance evaluation by simulating the modified source code elements and counting the data traffic on the bus (Page 2, Para 5, L1-3; Page 3, Fig. 1; Page 4, Para 1, L2-3).

13.5 As per the applicants' argument that "Raimi does not teach or suggest a software bus between the hardware and software elements of the simulation to exchange data traffic as required by claim 11; Raimi teaches that isolation between hardware and software elements are defined by "known" parameters; Adams does not overcome the shortcomings of the Tammema reference; Adams teaches sequential reading of lines of source code for syntax analysis; Adams does not teach or suggest a software bus between the hardware and software elements of the simulation to exchange data traffic as required by claim 11", the Examiner takes the position that Tammema teaches software modeling of the hardware and software elements of design for hardware/software co-simulation; the data transfer between the hardware elements and the software elements is modeled as part of the interface between the two; the bus in the software model is a software bus, as explained in Paragraph 13.4 above.

Conclusion

ACTION IS FINAL

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14. Applicant's arguments with respect to claim rejections under 35 USC § 103 (a) are not persuasive. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard, can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K. Thangavelu
Art Unit 2123
January 13, 2006


Paul L. Rodriguez 1/12/06
Primary Examiner
Art Unit 2125